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THE DERIVATION OF ANALYTICAL DESIGN EQUATIONS FOR BUILT–IN CURRENT SENSORS FOR USE IN IDDQ TESTING

BY
DAVID ARTHUR GREVE
B.S., University of Iowa, 1990

THESIS

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ABSTRACT

Iddq testing is a parametric test which uses quiescent power supply current monitoring to detect faults in CMOS circuits. One of the most interesting techniques for performing Iddq testing involves the use of built-in current sensors. Much of the previous work in the area of built-in current sensors, however, has centered on original current sensor designs. In fact, very little has been said concerning the issues associated with the actual implementation of these sensors. In this thesis, analytical design guidelines are developed which can be used by circuit designers to optimize the speed, resolution, and scalability of a variety of built-in current sensors. The development of these guidelines is based on a simple circuit analysis of the sensing device and it is supported with results from several Spice simulations.

This work is dedicated to the memory of my father, Gary Greve, who encouraged me in my quest for knowledge, and to my mother, Sally Greve, who taught me everything I needed to know.

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1. INTRODUCTION

Iddq testing is a parametric test which uses quiescent power supply current monitoring to detect faults in CMOS circuits. The usefulness of Iddq testing has been well established and a substantial amount of work has been published on the benefits of Iddq testing in general. Although there are a number of means available for performing Iddq testing, one of the most interesting techniques involves the use of built-in current sensors. Much of the previous work in the area of built-in current sensors, however, has centered on original current sensor designs. In fact, very little has been said concerning the issues associated with the actual implementation of current sensors. In the following chapters, analytical design guidelines are developed which can be used by circuit designers to optimize the speed, resolution, and scalability of a variety of built-in current sensors. The derivation of these guidelines is based on a simple circuit analysis of the sensing device and it is supported with results from several Spice simulations. Eventually these results will also be supported with data from a test chip specially designed to allow statistical evaluation of the impact of variations in the crucial parameters associated with sensor operation.

Following this introduction, some previous work in the field of built-in current sensors for use in Iddq testing is surveyed. After the survey of previous work, the basic circuit configuration of a built-in current sensor is described and the assumptions concerning this circuit are discussed. This leads into the circuit analysis performed in Chapter 2, which derives a set of equations linking the speed of the sensor to the basic parameters of the circuit. Results from these equations are then compared to actual Spice simulations, and the performance impact of each of the basic circuit parameters is discussed. Also considered is the impact of noise and parametric variations on the sensor performance. Chapter 3 takes these equations and derives a figure of merit for sensor designs, which is then employed in Chapter 4 on a simple example circuit to demonstrate both the utility of the figure of merit as well as the tradeoffs faced by the sensor designer. Chapter 5 concludes this thesis and reviews the material presented herein.

1.1 Previous Work

As mentioned earlier, much of the previous work in the area of built-in current sensors has centered on original current sensor designs. Even so, however, most of the proposed sensor designs operate in essentially the same manner; by inserting some type of sensing device into the power supply of the module under test to allow the current consumption of the module to be measured.

Wojcicch Maly and Phil Nigh appear to have been among the first to give serious consideration to the use of built-in current sensors (or BIC sensors) to perform Iddq testing. In one of their earlier works [1], a current sensor was proposed which used a diode connected BJT as a sensing element.

This design also included a very small transistor in parallel with the BJT. However, the utility of the parallel transistor during normal tester operation was never explored.

In a follow-up paper on this same basic sensor [2], Maly and Patyra mentioned the existence of a tradeoff between the module size, the current resolution, and the operating speed of the sensor. However, the specifics of this tradeoff were never fully developed, and it is this avenue, among others, which is more thoroughly explored in this thesis.

Shen, Daly, and Lo proposed an alternative design which expanded the role of the parallel MOS transistor [3]. It was suggested in their paper that the parallel MOS transistor be utilized as the primary sensing element, and that the diode should act only as a low impedance path for large switching currents. This appears to be a substantial deviation from Maly and Nigh, who apparently considered only the diode's exponential I/V curve in their analysis.

There have been several other designs proposed based on sensors composed only of MOS transistors [4]–[6]. In general, however, these designs would appear to suffer either from a lack of current-carrying capability during large transient currents or from a lack of resolution at low current levels. The drawbacks of such designs will be further examined in Chapter 4.

1.2 Basic Circuit Configuration

The basic configuration of the current sensors discussed throughout this thesis is shown in Figure 1.1. The module under test (MUT) is connected to a system ground only through a sensing device composed of a diode and an MOS transistor in parallel. The ground node of the module, no longer being tied directly to the system ground, becomes a floating, or virtual, ground. The diode, with its exponential I/V curve, provides a low impedance connection between the virtual ground node and the system ground during large transient currents. The transistor, on the other hand, provides a nonzero bias current at lower voltages to help decrease the settling time of the circuit. The virtual ground has an associated capacitance which must be overcome for the circuit to reach steady-state. After the virtual ground reaches some steady-state value, a sense amplifier compares the voltage on the virtual ground with a reference voltage to generate a pass/fail flag. If the virtual ground is greater than the reference, the module will fail the test. If the virtual ground is less than the reference, the module will pass.

The analysis performed on this configuration applies equally well to modules with sensor elements located in the power node, and many of the results derived for the parallel diode/transistor case are reducible to the degenerate cases where only either a diode or a transistor is used as a sensing element.

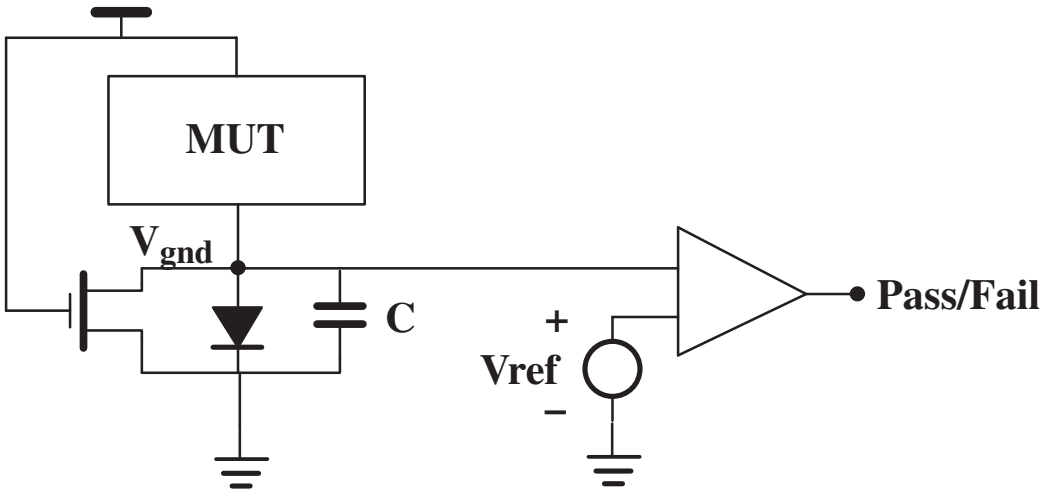

Figure 1.1 Basic current sensor configuration. Note the module under test (MUT), virtual ground node (V_{gnd}) formed by the parallel diode/transistor sensor element, effective capacitance (C), reference voltage (Vref) and sense amplifier which produces a Pass/Fail flag.

1.3 Model Assumptions and Approximations

It is assumed throughout this thesis that the clock cycle of the circuit under test can be divided into two subcycles. The first part of the cycle is the switching cycle, defined as that portion of the clock cycle during which the inputs to the module change and the logical output is generated. It is assumed that the inputs will have completely propagated through the module prior to the end of the switching cycle. The testing cycle, on the other hand, is that portion of the clock cycle during which the inputs to the module remain fixed. During this cycle, the sensor waits for the circuit to reach a steady-state condition and then, at the end of the cycle, the sensor samples the virtual ground and determines the pass/fail status of the module.

The current flow through the module under test is, in general, very difficult to model accurately. For the purpose of this analysis, therefore, this current is assumed to be composed of three basic components : switching current, leakage current, and error current.

The switching current, or I_{sw}, is that current associated with circuit activity within the module under test. As gates within the module change state, large current spikes appear during those short periods of time when both the p and n networks of the gates are simultaneously conducting. These spikes are followed by decaying exponential current waveforms, which result as the charge stored

on the capacitive output loads discharge through the conducting networks of the gates. The duration of these exponential waveforms should be closely related to the fall times of the gates making up the module under test. In fact, it is expected that the switching currents will have nearly died out within a few nanoseconds after the last gate in the module transitions.

This type of circuit activity, however, is very difficult to model accurately. This is due in part to the fact that the current waveforms will depend not only on the particular module under test, but also on the specific inputs to that module. Fortunately it is not necessary to know the specific time value of the switching current for the purposes of this analysis. In fact, it is the impact of the switching current on the virtual ground voltage, rather than the switching current itself, which is of interest. Therefore, rather than trying to model the switching activity of the module under test, it is simply assumed that the gates within the module can switch at any time up until the very end of the switching cycle. It is further assumed that the current spike generated by such switching activity will be very large and that the virtual ground voltage resulting from such a spike will also be very large. This analysis, therefore, will simply assume that the virtual ground voltage at the beginning of the testing cycle (at the end of the switching cycle) is very large. Such an assumption should result in a worst-case settling time for the virtual ground voltage. The Spice simulations discussed in Chapter 2 incorporate this assumption by simply modeling the switching current as a step function with a very large magnitude which turns on at the start of the switching cycle and which turns off at the beginning of the testing cycle.

After the testing cycle begins, the module current is assumed to be a dc current composed only of the module leakage current and any resulting error current, collectively referred to as I_e. Leakage current is that current which normally flows through a module under dc conditions. This current is made up of essentially three components: junction leakage current, subthreshold leakage current, and gate leakage current. The junction leakage current is a current associated with the reverse biased p–n junctions in the circuit. The junctions in question include reverse biased well to substrate, drain to well, and source to well junctions. The second component of the leakage current is the subthreshold leakage current. Subthreshold leakage current is simply that current which flows through a transistor which is considered to be off. The final component is gate leakage current, a current due simply to the finite (albeit large) resistance of a transistor gate. The portion of the module current, I_e, due to leakage current will hereafter be referred to as I_{eo}.

The leakage current is expected to vary proportionately with the size of the module. However, even for relatively large modules, the magnitude of this leakage current is expected to be overshadowed in the presence of the third and final component of the module's current consumption, the error current. Error current is that current which results from shorts, opens, or other faults within the circuit. For the purposes of this analysis, the error current is considered to

take on some constant value, independent of the voltage on the virtual ground. The module current, I_e, in the presence of errors is denoted as I_{err}[1].

The impact of these approximations to the module's current consumption can be summarized as follows. During each cycle, as the module switches, the voltage on the virtual ground will become very large and the current through the diode will dominate the current flow from the virtual ground. When the module stops switching, the voltage on the virtual ground will at first drop quite quickly as the charge stored on the capacitance of the virtual ground is drained away by the exponential diode current. However, as the voltage on the virtual ground nears zero, there will be some voltage at which the current through the bypass transistor will begin to dominate that of the diode. In this region the voltage will drop more slowly until it decays to some dc value, not necessarily zero given a nonzero value of I_e. The rate at which the virtual ground decays to its dc value is dependent on several factors, but perhaps the most important is the effective capacitance of the virtual ground.

The effective capacitance of the virtual ground is simply that capacitance which must be overcome to charge or discharge the virtual ground node. This capacitance can include the routing capacitance of the virtual ground node, the junction capacitances of well to substrate and/or source to well junctions connected to the virtual ground node, the sensor diode junction capacitance, and finally the load capacitance seen by each device in the module which drives its output low. This final component of the effective capacitance is obviously dependent on the state of the module under test. However, for sufficiently large and/or random modules, this dependence should be negligible.

[1]Note that this term includes the module leakage current, I_{eo}

2. CIRCUIT ANALYSIS

By observing a simplified diagram of the basic sensor configuration of Figure 2.1, it is possible to identify those current contributions which will most significantly impact the voltage on the virtual ground.

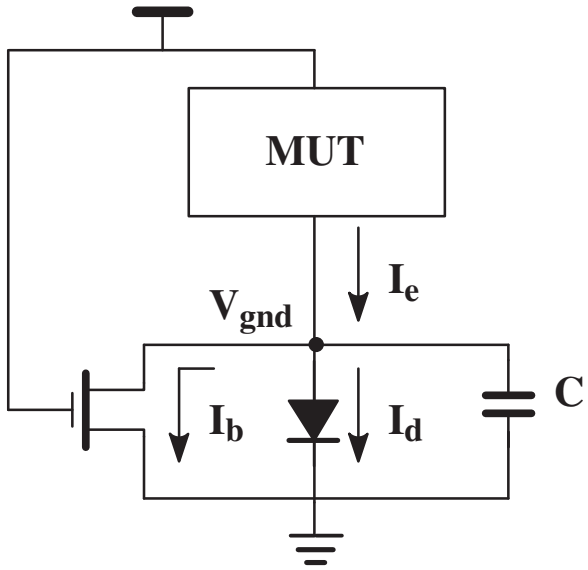

Figure 2.1 Circuit model used in analysis. Note diode current (I_d), bias transistor current (I_b), module current (I_e), and effective capacitance of virtual ground (C).

The current contribution of the diode can be expressed as

$$I_d = I_s * \left(\exp\left[\frac{v}{v_t}\right] - 1 \right) \simeq I_s * \exp\left[\frac{v}{v_t}\right] \tag{2.1}$$

where I_s is the diode saturation current and v_t represents the product of the thermal voltage, kT/q, and the diode thermal coefficient, n. The current contribution of the bias transistor, on the other hand, can be expressed as

$$I_b = k * \left(\left(V_{gs} - V_{th}\right) v - \left(\frac{1}{2}\right) v^2 \right) \simeq 4k * v - \frac{k}{2} * v^2 \tag{2.2}$$

where

$$k = \left(\frac{W}{L}\right)\left(\frac{u_n * \epsilon_{ox}}{t_{ox}}\right) \tag{2.3}$$

and where (V_{gs} – V_{th}), the gate to source voltage minus the threshold voltage, is approximated by (5 – 1) or 4 volts.

To solve for the delay of the current sensor, the differential equation governing the voltage on the virtual ground must first be evaluated. This equation takes the following form

$$I_s * \exp\left[\frac{v}{v_t}\right] + 4k * v - \left(\frac{k}{2}\right) * v^2 - Ie = -C\left(\frac{dv}{dt}\right) \tag{2.4}$$

This differential equation can be solved for the length of time it takes for the virtual ground to decay from its initial voltage to some final voltage. To do this, the variables t and v are separated and the two sides of the equation are integrated over the ranges of interest, t from zero to t and v from V_0 (the voltage at the beginning of the test cycle) to v, the voltage of interest. Separation of the differential equation yields

$$\int_0^t d\tau = -C \int_{V_0}^{v} \frac{dv}{I_s * \exp\left[\frac{v}{v_t}\right] + 4k * v - \left(\frac{k}{2}\right) * v^2 - I_e} \tag{2.5}$$

This equation cannot be solved explicitly as it stands. However, a closed form solution can be obtained if the integral over v is split into two regions and (2.5) is approximated by two simpler equations. It is easy to see that for large values of v, the exponential term dominates the denominator. This observation allows (2.5) to be approximated as

$$\int_0^t d\tau \simeq -C \int_{V_0}^{v} \frac{dv}{I_s * \exp\left[\frac{v}{v_t}\right] + I_1} \tag{2.6}$$

where the term I_1 is simply a correction factor which accounts for the impact of all of the current contributions outside the diode itself (the module current and the bias transistor current) over the voltage range of interest. Obviously the accuracy of this approximation depends on the value chosen for I_1. However, I_1 also depends on the voltage range over which this approximation is to be used. Therefore, it is important to first bound the range over which this approximation will

be used. Equation (2.6) turns out to be a good approximation to (2.5) up to the inflection point of (2.6). The inflection point, V_I, can be determined by taking the second derivative, setting it equal to zero, and solving for V_I

$$\frac{d^2}{dV_1^{\,2}}\left[\frac{1}{I_s * \exp\left[\frac{V_1}{V_t}\right] + I_1}\right] = 0 \tag{2.7}$$

which gives

$$V_1 = v_t * \ln\left[\frac{I_1}{I_s}\right] \tag{2.8}$$

As mentioned previously, I_I is a correction factor which accounts for the impact of the module current and the bias transistor current over the voltage range of interest. For voltages much greater than V_I the exponential term dominates the equation. Thus, the impact of the other current contributions for voltages much greater than V_I is negligible. In the region of V_I, however, the other current contributions become comparable to the exponential diode current. Thus, it is the current contributions in the region of V_I which will have the greatest impact on the accuracy of this approximation. For this reason, a good value for I_I is simply the current contributions of the module and the bias transistor at V_I. A reasonable value for I_I can thus be found from

$$I_1 = 4k * V_1 - \left(\frac{k}{2}\right) * V_1^2 - I_e \tag{2.9}$$

Equations (2.8) and (2.9) form a pair of simultaneous equations which must be solved before the values of I_I and V_I can be determined. An explicit solution to this system of equations does not exist, although one can be found numerically. However, for the sake of simplicity, a first approximation to I_I could be

$$I_{1(0)} = 4k - I_e \tag{2.10}$$

If this value is negative, the diode current will dominate for all voltages of interest and the inflection point will not exist. If not, however, an approximate inflection point can be calculated from (2.8) as

$$V_{1(0)} = v_t * \ln\left[\frac{4k - I_e}{I_s}\right] \tag{2.11}$$

A more accurate value of I_1 can now be determined. If an inflection point exists, then $V_{1(0)}$ can be used in (2.9) to determine I_1 and a more accurate value for V_1 can be calculated by substituting the resulting value of I_1 into (2.8). If, however, an inflection point does not exist, then the voltage of interest, v, should simply be used in (2.9) to calculate I_1.

Once I_1 has been determined, (2.6) can be integrated to give

$$t = -C\left[\frac{v}{I_1} - \left(\frac{v_t}{I_1}\right) * \ln\left[I_1 + I_s * \exp\left[\frac{v}{v_t}\right]\right]\right]_{v_0}^{v} \tag{2.12}$$

which evaluates to

$$t = \left(\frac{C * v_t}{I_1}\right)\left[\ln\left[\frac{I_1 + I_s * \exp\left[\frac{v}{v_t}\right]}{I_1 + I_s * \exp\left[\frac{V_0}{v_t}\right]}\right] + \frac{V_0 - v}{v_t}\right] \tag{2.13}$$

Equation (2.13) can be rewritten as

$$t = \left(\frac{C * v_t}{I_1}\right)\ln\left[\frac{\left(\exp\left[\frac{V_0}{v_t}\right]\exp\left[-\frac{v}{v_t}\right]\right)\left(I_1 + I_s * \exp\left[\frac{v}{v_t}\right]\right)}{I_1 + I_s * \exp\left[\frac{V_0}{v_t}\right]}\right] \tag{2.14}$$

or, equivalently, as

$$t = \left(\frac{C * v_t}{I_1}\right)\ln\left[\frac{I_1 \exp\left[-\frac{v}{v_t}\right) + I_s * \exp\left[\frac{V_0}{v_t}\right]}{I_1 + I_s * \exp\left[\frac{V_0}{v_t}\right]}\right] \tag{2.15}$$

which, for sufficiently large values of V_0, reduces to

$$t = \left(\frac{C * v_t}{I_1}\right)\ln\left[\frac{I_1}{I_s}\exp\left[-\frac{v}{v_t}\right] + 1\right] \tag{2.16}$$

Equation (2.16) gives the maximum amount of time it can take for the virtual ground to decay to v volts following a circuit transition. However, per previous assumptions, this solution is valid only for $V_1 < v$. If V_1 from (2.8) does not exist (i.e., if $I_1 < 0$), then (2.16) is valid only for values of v such that

$$\frac{I_1}{I_s}\exp\left[-\frac{v}{v_t}\right] + 1 > 0 \tag{2.17}$$

or, equivalently,

$$v > v_t * \ln\left[-\frac{I_1}{I_s}\right] \tag{2.18}$$

For simplicity, (2.18) can be combined with the inflection point calculated in (2.8) to establish the lower limit on v in (2.16) as ($V_1 < v$) where

$$V_1 = v_t * \ln\left[\frac{|\, I_1 \,|}{I_s}\right] \tag{2.19}$$

Assuming that a solution exists for voltages below V_1, the maximum time (T_1) to reach the threshold (V_1) will simply be (2.16) evaluated at $v = V_1$. A new approximation for (2.5) must then be used to find the time it takes the virtual ground to decay from V_1 to its final voltage. While (2.6) was derived by assuming that the diode current dominated the denominator, a solution for v less than V_1 can be derived by assuming that the current contribution of the diode can be neglected.[2] In this case, (2.5) can be rewritten as

$$\int_{T_1}^{t} d\tau \simeq -C \int_{V_1}^{v} \frac{dv}{4k * v - \left(\frac{k}{2}\right) * v^2 - I_e} \tag{2.20}$$

or, equivalently,

$$\int_{T_1}^{t} d\tau = -\left(\frac{2C}{k}\right) \int_{V_1}^{v} \frac{dv}{(r_1 - v)(r_2 - v)} \tag{2.21}$$

[2]A more accurate solution can be obtained by retaining an exponential contribution. See Appendix A.

where r_1 and r_2 are defined as

$$r_1 = 4 - \sqrt{16 - 2\frac{I_e}{k}} \tag{2.22}$$

$$r_2 = 4 + \sqrt{16 - 2\frac{I_e}{k}} \tag{2.23}$$

Equation (2.21) can be integrated to give

$$t = T_1 + \left(\frac{2C}{k\,(r_1 - r_2)}\right)\Big[\Big(\ \ln\big[v - r_1\big] - \ln\big[r_2 - v\big]\ \Big)\Big]_{V_1}^{v} \tag{2.24}$$

which evaluates to

$$t = T_1 + \left(\frac{2C}{k\,(r_1 - r_2)}\right)\left\{\ \ln\left[\frac{v - r_1}{V_1 - r_1}\right] - \ln\left[\frac{r_2 - v}{r_2 - V_1}\right]\ \right\} \tag{2.25}$$

and which can be further simplified to

$$t = T_1 + \left(\frac{2C}{k\,(r_2 - r_1)}\right)\ln\left[\frac{(v - r_2)(V_1 - r_1)}{(v - r_1)(V_1 - r_2)}\right] \tag{2.26}$$

This equation represents the time required for the virtual ground node to decay to some voltage, $v < V_1$. However, this equation, too, is valid only over a specific range of v. Note that r_1, as given in (2.22), represents a root of the current equation used in (2.20). As a root, it also represents a dc operating point of the circuit and therefore the voltage on the virtual ground will never drop below r_1. Thus, (2.3) can be considered to be valid only for ($r_1 < v < V_1$).

2.1 Verification and Analysis of Delay Equations

In order to verify the correctness of the delay equations, the simple circuit shown in Figure 2.2 was constructed and simulated in Spice. The simulations which will be presented here result from a circuit with the basic characteristics shown in Table 2.1.

These simulations show the results of varying one of each of the parameters listed in Table 2.1 while leaving the others at their default value. This was done to verify the individual contributions of these parameters in the derived equations as well as to evaluate the relative impact that the various circuit parameters have on the sensor performance. Plots of the values expected from the

delay equations are included along with the Spice results for each circuit.[3] Because of the accuracy of the derived results, however, only very close observation will reveal that the following figures contain two versions of each curve – one resulting from the Spice simulation and the other from the evaluation of the delay equations.

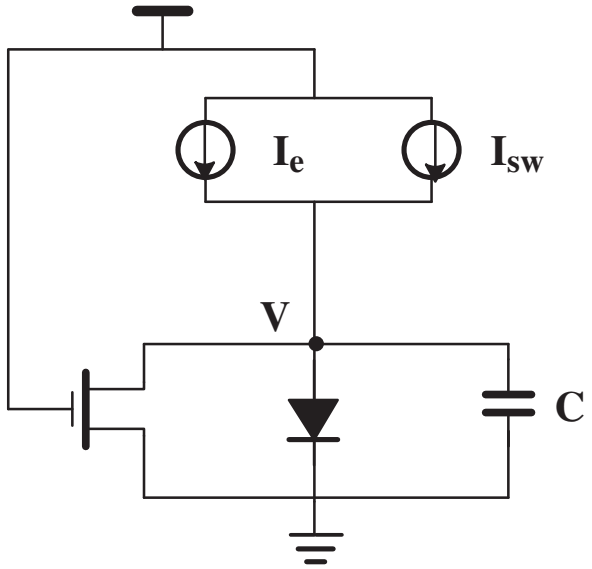

Figure 2.2 Spice circuit used to verify delay equations. The circuit includes the module dc current, I_e, and the module switching current, I_{sw}.

Table 2.1 Properties of basic Spice circuit

	I_s	C	k	I_e	V_0
Base Circuit	1e–16 A	10 pF	80 uA/V^2	40 uA	.85 V

Figure 2.3 shows the impact of variations in *C* on the delay of the sensor. As expected from the original differential equation, the sensor delay is essentially linear in *C* (note the time it takes to reach 0.4 V in each case). Since the value of *C* should be nearly linear in the number of gates

[3]The equations used in generating these plots used the more accurate version of the delay equations derived in Appendix A.

in a module, it is expected that the sensor delay will also be linear in the number of gates in the module. This result has been previously reported in [2], though in a much more informal manner.

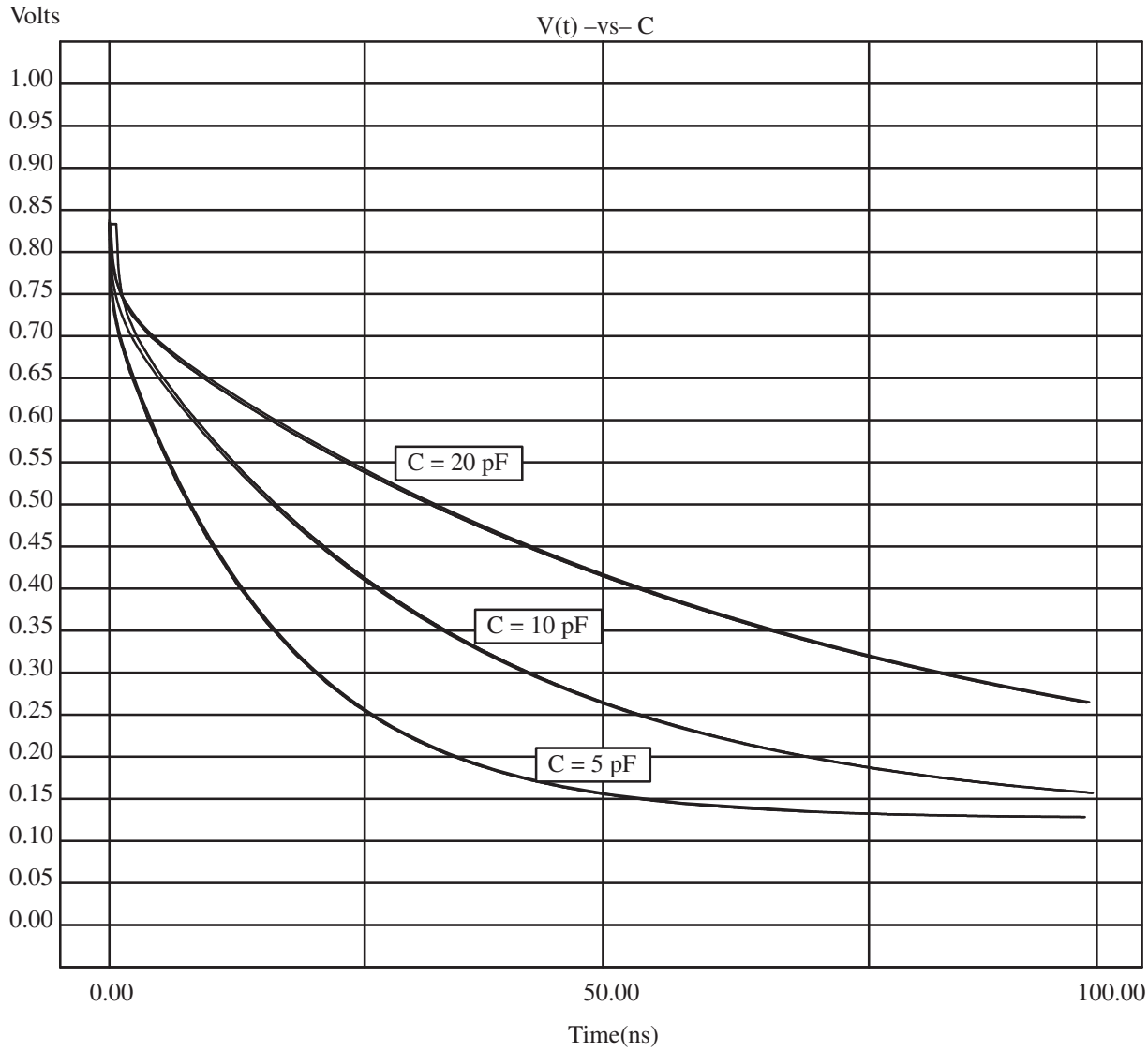

Figure 2.3 Virtual ground delay over variations in C.

The impact of the bias current is demonstrated in Figure 2.4. Note that when $k = 0$ uA/V^2, the virtual ground never falls below 0.69 V. This is simply because the dc operating point of the circuit is near 0.7 V. As k is increased, however, the dc operating point of the circuit is reduced until it is below 0.1 V for $k = 120$ uA/V^2. Although the circuit actually takes longer to reach its dc operating point as k is increased, it should be noted that, for an arbitrary voltage above the dc

operating point, the circuit delay is actually reduced as k is increased. It is this fact, among others to be discussed later, that makes the bias transistor an appealing addition to the sensor circuit.

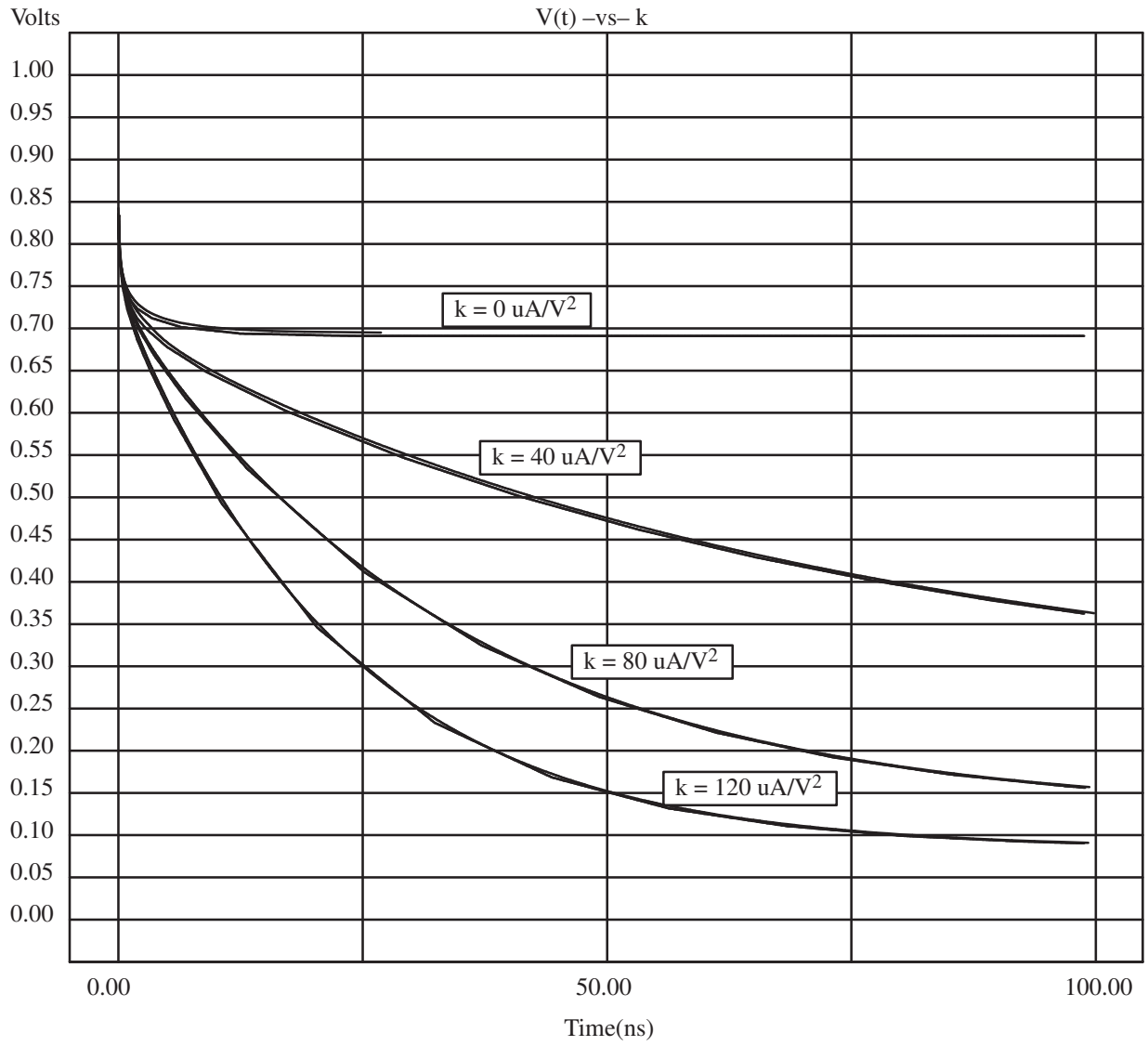

Figure 2.4 Virtual ground delay over variations in k.

Figure 2.5 shows the sensor delay under various values of the module current, I_e. Note that, as the module current increases, so does the time it takes for the virtual ground to decay to a given voltage. Actually, the same principle is at work here as in the case of the bias current, only in reverse. As the module current increases, so does the dc operating point. Thus, although the circuit takes less time to reach steady–state, it takes longer to reach any arbitrary voltage.

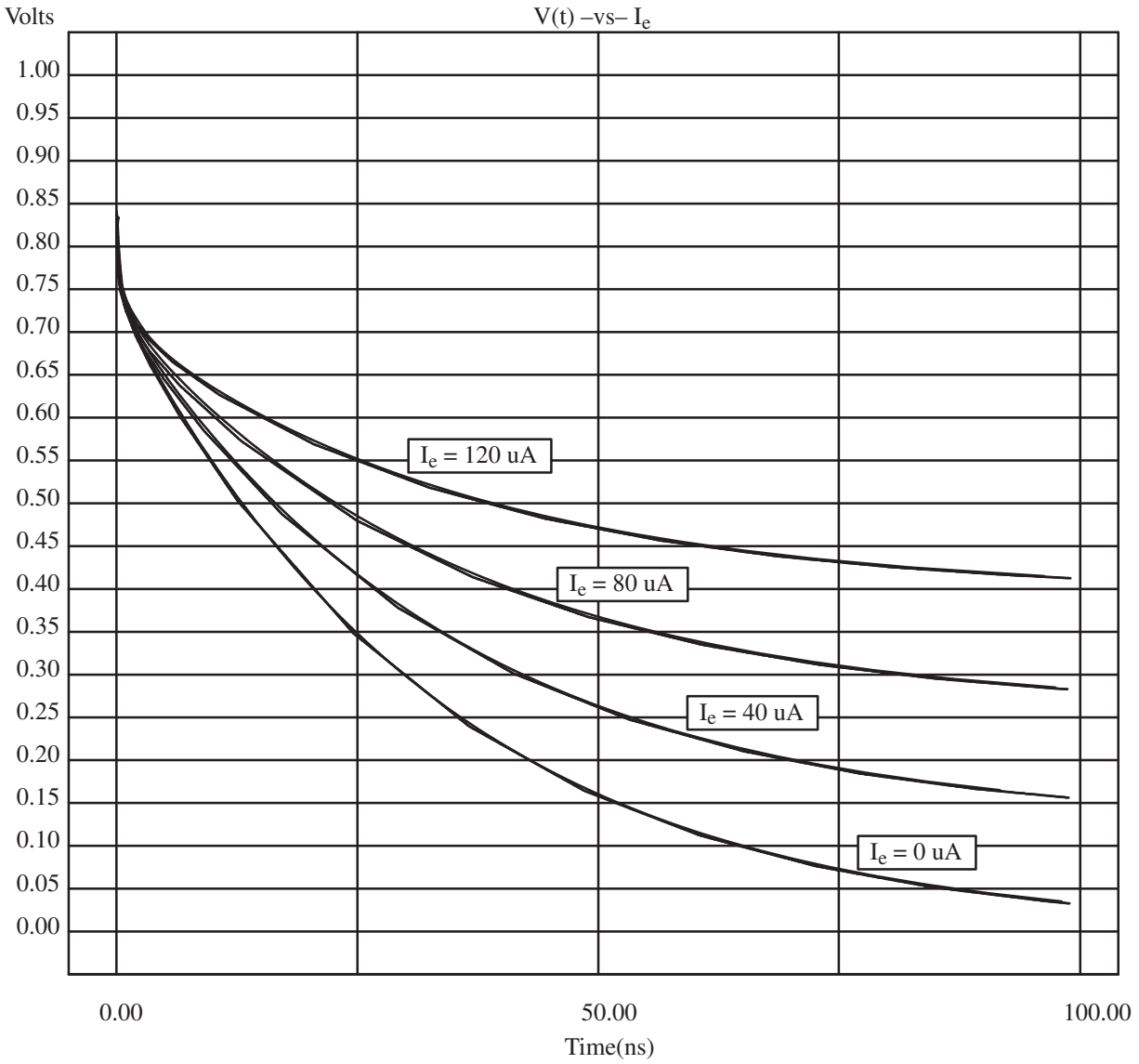

Figure 2.5 Virtual ground delay over variations in I_e.

Figure 2.6 shows the impact of variations in the diode saturation current, I_s. Note that the basic slope of the curves is insensitive to variations in I_s. In fact, the circuit delay itself is relatively insensitive to the diode saturation current. This can be seen by comparing the portion of the delay associated with the diode, T_1, with the total delay, t, in Table 2.2. For sufficiently small values of v, the portion of the delay which can be attributed to the diode is very nearly negligible when compared to the delay due to the transistor. The advantage of large I_s lies in its impact on the value of V_1. Large variations in I_s can result in significant differences in V_1, and as V_1 becomes smaller,

the virtual ground has less distance to go before reaching *v*, ultimately reducing the delay of the sensor.

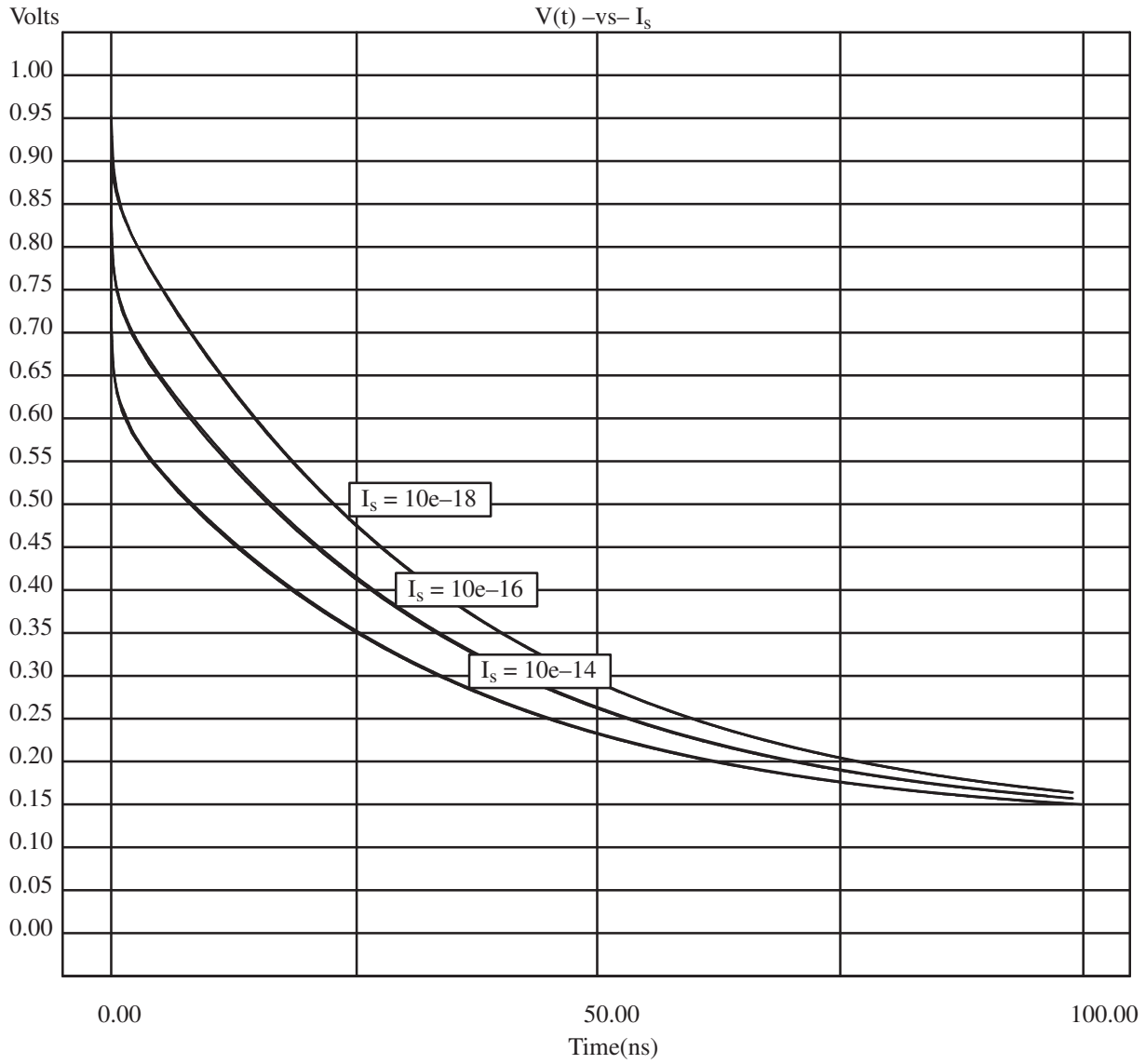

Figure 2.6 Virtual ground delay over variations in I_s.

With I_s (measured in amps per square micrometer) being constant for a given process, only an increase in diode area will result in an increase in the value of I_s (in amps). It is unlikely, however, that a significant decrease in sensor delay could be obtained by simply increasing the area of the sensor diode. In fact, since the capacitance of the junction diode is proportional to the area of the diode, and since the delay of the sensor is linearly dependent on the capacitance of the virtual

ground, there will be a point beyond which increasing the area of the diode will actually increase the delay of the sensor.

Table 2.2 Components of total circuit delay. All voltages are listed in volts, all currents in amperes, and all times in nanoseconds.

				t(v)		
		V_1	T_1	.6	.4	.2
I_S	1e–18	.86	0.69	15.0	33.0	77.0
	1e–16	.73	1.10	8.4	27.0	70.0
	1e–14	.60	1.50	1.6	19.0	62.0

One possible means of skirting this limitation would be the use of Schottky diodes, which typically have a much larger value of I_s (in amps per square meter) than junction diodes. Schottky diodes also have the advantage of negligible forward bias capacitance. Thus, using Schottky diodes, the sensor speed should always improve with increases in diode area.

Another advantage of increased I_s may lie in reduced power supply degradation. Although the issue of the logical delay of a module under test is not directly addressed by this thesis, there is a relationship between the voltage degradation of the power supplies and the delay of the module under test. It has been reported in a number of previously published works that the inclusion of the sensor element in the power supply of a module results in degradation of the module's performance [1],[2].

Figure 2.7 shows the delay of a module composed of a string of 96 inverters under normal conditions and in the presence of a sensor diode with two different values of diode saturation current. Note that, for larger values of I_s, the degradation of the virtual ground voltage is slightly less and that the performance of the module is slightly better. This result would seem to support the idea that larger diodes, or diodes with larger values of I_s, are the preferred sensor elements.

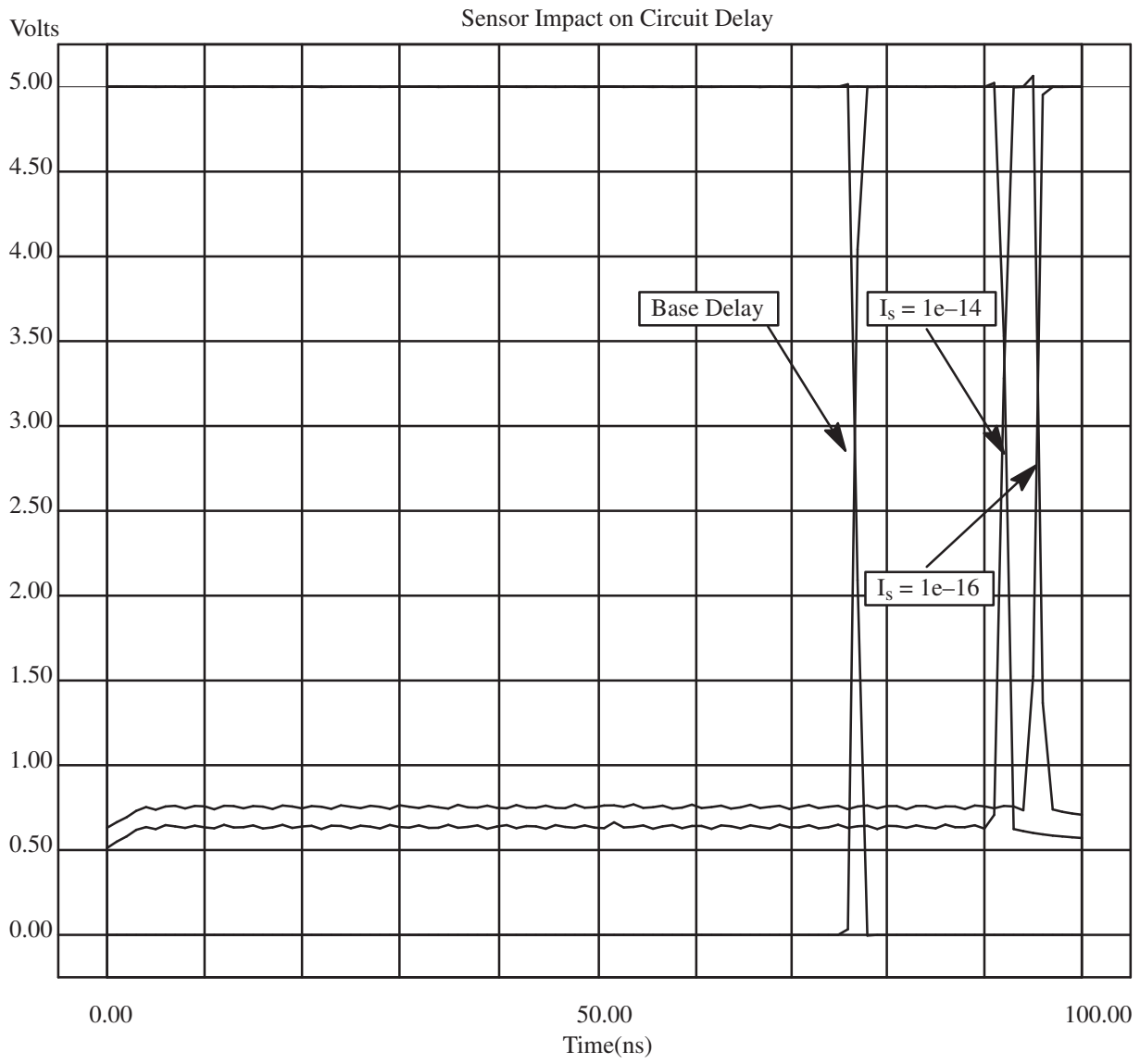

Figure 2.7 Sensor impact on circuit's logical delay.

2.2 Dealing with Noise and Uncertainty

In the previous section the equations governing the voltage on the virtual ground node were derived and verified using Spice. However, although these equations are nearly exact in an ideal environment, they may not apply well to an environment wrought with uncertainty and noise, an environment such as digital power supply. Before these equations can be used to design a current sensor, then, some technique must be employed to quantify the impact of uncertainty and noise.

The easiest method of dealing with this problem is to simply define margins to account for possible deviations from an expected value. This is the technique which will be employed in this thesis. Given that there exists uncertainty in the values of C, I_s, v_t, or k, a worst-case analysis can be performed on the extreme values of these parameters to derive results which will take into account these parametric uncertainties. A worst-case maximum delay can be derived using the maximum values of C and v_t and the minimum values of I_s and k. A worst-case minimum delay, on the other hand, can be determined using the minimum values of C and v_t and the maximum values of I_s and k.

It should be possible to deal with most of the remaining uncertainty in a sensor design by defining switching thresholds for the sensor itself and by establishing a lower and upper limit on the length of the testing cycle. Of the two, perhaps the most difficult is determining the switching thresholds of the sensor.

The switching thresholds of the sensor are defined as those virtual ground voltages above or below which the sensor is essentially guaranteed to signal a failure or a pass. These thresholds are influenced by a number of factors. One important factor which contributes to uncertainty in the switching thesholds is uncertainty associated with the voltage reference. If the voltage reference is generated on-chip, it will be subject to uncertainty due mainly to process variations, but it can also be impacted by noise on the power supplies as well as coupling noise from nearby circuitry. An externally generated reference might be more accurate, but it, too, would also be subject to coupling noise as it is routed over the circuity on the chip.

The switching thresholds of the sense amplifier itself must also be considered when calculating the sensor switching thresholds. Due to small variations in transistor sizings and differences in node capacitances, the sense amp will have built-in switching thresholds. Although process variations can be modeled in Spice to determine the expected thresholds, results from actual physical devices may provide more accurate information concerning the sense amplifier's resolution. Also, although noise on the sensor power supply should essentially be common mode in nature, input capacitance asymmetries may cause common mode noise on the power supplies to appear as differential noise on the sensor inputs, resulting in further degradation of the resolution of the sense amplifier.

Finally, uncertainty associated with the voltage on the virtual ground node itself will impact the switching thresholds as well. Although the delay equations derived above appear quite accurate, the virtual ground will still be subject to noise both through coupling with other digital circuits and, more importantly, through its diode/transistor connection to the power supply. The combination of the sensor diode and the capacitance of the virtual ground forms a voltage rectifier, which will tend to drain the voltage on the virtual ground node during each negative transition of the system

ground node. This effect will be offset somewhat in dc conditions by the bias transistor, which will tend to pull the virtual ground node back up as the system ground node returns to a normal (or super normal) voltage. Even so, the impact of power supply noise still remains.

Combining all of these factors into quantities which can be used in the design process results in the following equations. The upper switching threshold can be defined as

$$V_{th+} = V_r + V_{sf+} \tag{2. 27}$$

and the lower switching threshold as

$$V_{th-} = V_r - V_{sf-} \tag{2. 28}$$

where V_r in the above two equation is the expected value of the voltage reference and V_{sf+} and V_{sf-} are voltage safety factors required to compensate for the aforementioned uncertainties with an acceptable degree of confidence.

A useful quantity which can be derived from the above two equations is the required voltage margin (*RVM*) of the circuit, defined as

$$RVM = (V_{th+} - V_{th-}) = (V_{sf+} + V_{sf-}) \tag{2. 29}$$

The RVM is simply the voltage margin which must exist between the upper and lower switching thresholds in order to allow for the distinction between faulty and fault-free modules.

Once the switching thresholds for the circuit have been determined, all that remains is to establish limits on the test cycle length. The minimum test cycle length, T_{min}, is defined as the minimum amount of time that the circuit will have to settle between the end of the switching cycle and the end of the testing cycle. A good value for T_{min} may simply be the difference between the total cycle time and the worst-case logical delay of the module under test (the maximum switching cycle period), perhaps minus some safety factor.

The maximum tester period, T_{max}, on the other hand, is defined as the maximum possible period of the tester cycle. Whereas a reasonable limit for the minimum test cycle length is quite easy to determine, it is much more difficult to establish a useful upper limit on the test cycle length. To do so requires knowledge of the actual current waveform of the module under test, as well as the behavior of the module inputs. The easiest solution to this problem is to simply define the maximum cycle length as being infinite. However, it turns out that the resolution of the sensor may be improved by establishing a less conservative upper limit on the test cycle length.

3. SENSOR DESIGN EQUATIONS

The design of a current sensor is essentially defined by the following three parameters : the error current resolution, the speed of operation, and the size of the module under test. These three factors form the basis of the sensor design space, where the choosing of any one of the parameters results in some tradeoff between the other two. The design space for a given sensor can be visualized as a graph of the time/voltage characteristics of the virtual ground under variations of some design parameter. Vertical lines in such a graph can be used to represent the two switching thresholds, V_{th+} and V_{th-}, and horizontal lines can be be included at T_{min} and T_{max} to model the bounds on the test cycle time.

For a circuit design to have even marginal utility as an Iddq sensor, there are a couple of basic requirements which must be met. The first is that there must exist worst-case maximum time curves which fall below the point (T_{min}, V_{th-}) in the design space. In fact, given that the leakage current of the module is expected to contribute some nonzero component, I_{eo}, it should at least be true that the curve representing $I_e = I_{eo}$ pass below (T_{min}, V_{th-}). This is a requirement because curves which lie below this point represent circuits which will pass the Iddq test. These circuits will pass because, even with the shortest test cycle time, the voltage on the virtual ground is guaranteed to fall below the lower switching threshold, V_{th-}, before the end of the cycle. If, for a given design, no curves fall below this point, there is no guarantee that the circuit will ever pass an Iddq test.

A second requirement is that there must exist worst-case minimum time curves which fall above the point (T_{max},V_{th+}) in the design space. In fact, to detect Iddq faults of magnitude greater than I_{err}, the curve representing $I_e = I_{err}$ must lie above (T_{max}, V_{th+}). This is a requirement because curves which lie above this point represent those circuits which will fail the Iddq test. These circuits will fail because the voltage on the virtual ground will never fall below V_{th+}, even given the longest test cycle time. If this requirement is not met, there would be no guarantee that the circuit would ever fail an Iddq test when $I_e = I_{err}$. It is interesting to note that, for the case of T_{max} equal to infinity, only those circuits whose dc operating point is above V_{th+} are guaranteed to be detected as faulty. However, because there are some circuits whose dc operating point is below V_{th+}, but which would lie above the intersection of V_{th+} and some T_{max}, it turns out that the resolution of the sensor can be improved by establishing an upper bound on the test cycle.

By observing the design space of a circuit, it is possible to visually determine the minimum detectable error current and the maximum allowable value of I_{eo}. Figure 3.1 shows an example of a circuit design space. Note that, for this circuit, values of I_e greater than 120 uA will be detected as Iddq faults, whereas values of I_e less than 20 uA will allow the circuit to pass as fault-free.

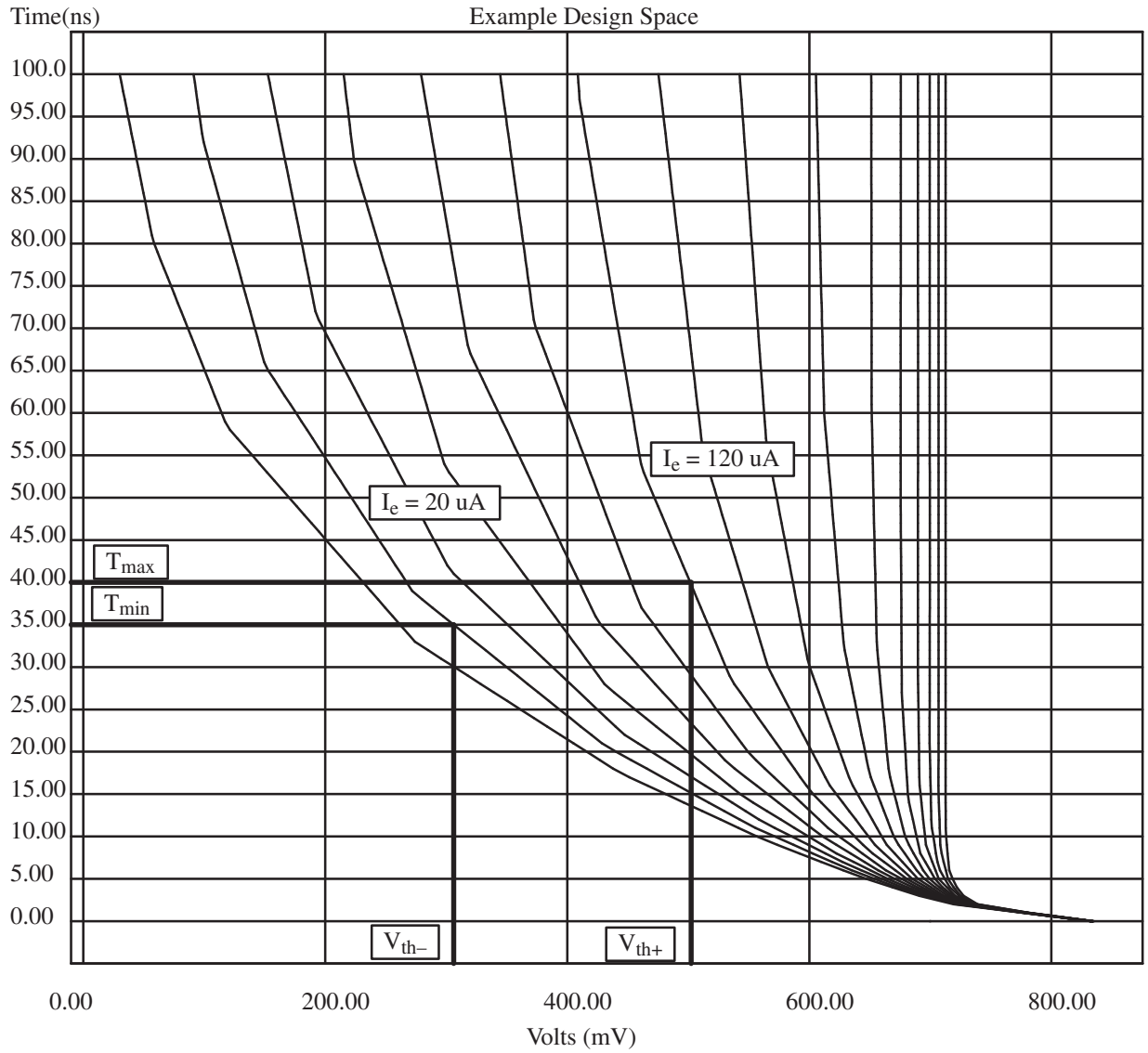

Figure 3.1 An example design space. Note T_{min} = 35 ns, T_{max} = 40 ns, V_{th-} = 0.3 V, and V_{th+} = 0.5 V. Note also that the curves representing I_e = 20 uA and I_e = 120 uA have been so indicated.

However, while plots of the sensor design space are informative to look at, they aren't particularly useful when it comes to optimizing a design. What is needed is some means of relating the parameters in the delay equations to the tolerances represented by the switching thesholds and the minimum and maximum test cycle times. This turns out to be possible if the delay equations are rearranged to represent *v* as a function of *t*, rather than *t* as a function of *v*. Doing so for (2.16) results in

$$v(t) = -vt * \ln\left[\frac{I_s}{I_1}\left[\exp\left[\frac{t * I_1}{C * v_t}\right] - 1\right]\right] \quad (3.1)$$

which is valid for ($V_1 < v$). Equation (2.26) can also be solved for v in terms of t, yielding

$$v(t) = \frac{(V_1 - r_2) * E * r_1 - (V_1 - r_1) * r_2}{(V_1 - r_2) * E - (V_1 - r_1)} \quad (3.2)$$

where

$$E = \exp\left[\frac{k\,(t - T_1)(4 - r_1)}{C}\right] \quad (3.3)$$

and which is valid from ($r_1 < v < V_1$).

The reason for deriving these equations is that they can now be used to relate T_{min}, T_{max}, V_{th+}, V_{th-}, and *RVM* to the physical circuit parameters used in the delay equations. This relationship can then be used to establish a measure of circuit "goodness" which can subsequently be used to optimize a given design.

For example, (T_{min}, V_{th-}) represents a point of interest in the design space of a sensor because it is hoped that the curve representing $I_e = I_{eo}$ lies at or below this point. By making the substitutions $I_e = I_{eo}$ and $t = T_{min}$ in (3.1) and (3.2), it is possible to determine the value of the lower switching voltage,

$$V_{sw-} = v(t) \Big|_{t = Tmin,\ Ie = Ieo} \quad (3.4)$$

which is simply the voltage on the virtual ground node at the end of the minimum length test cycle. If the calculated value of V_{sw-} is less than V_{th-}, then module currents of I_{eo} or less are guaranteed to pass the Iddq test.

In a similar manner, an expression for the upper switching voltage, V_{sw+} can be derived and compared to the upper switching threshold, V_{th+}, by setting $I_e = I_{err}$ and $t = T_{max}$.

$$V_{sw+} = v(t) \Big|_{t = Tmax,\ Ie = Ierr} \quad (3.5)$$

If the calculated value of V_{sw+} is greater than V_{th+}, then module currents of I_{err} or more are guaranteed to be detected as Iddq faults by the sensor.

It is simple to include the tolerances of the various circuit parameters in these expressions as well. The worst-case value of V_{sw-} will occur when I_s and k are at their minimums and C and v_t are at their maximums. Likewise, the worst-case value of V_{sw+} will result from the minimum values of C and v_t and the maximum values of I_s and k.

A figure of merit for an Iddq sensor design can now be defined as the available voltage margin, or *AVM*, which is simply the voltage difference between V_{sw+} and V_{sw-}

$$AVM = (V_{sw+} - V_{sw-}) \tag{3.6}$$

The *AVM* is the voltage which is guaranteed to separate a faulty module and a fault-free module for a given sensor design. The available voltage margin (*AVM*) of a design can then be compared to the required voltage margin (*RVM*) to determine whether a given design can meet the design specifications. As long as the *AVM* is greater than the *RVM*, it can be said that the design is feasible given an appropriate voltage reference. If, however, the *AVM* is less than the *RVM*, there is no guarantee that the sensor will both detect faulty modules and pass fault-free modules.

Assuming that the switching thresholds are symmetrical, an expression for an appropriate voltage reference can be calculated from

$$Vr = \frac{V_{sw+} + V_{sw-}}{2} \tag{3.7}$$

These equations can now be used to optimize a sensor design or to make tradeoffs between circuit size, testing cycle length, and error current resolution by providing feedback on how design changes impact the available voltage margins of the sensor in an uncertain environment.

4. USING THE SENSOR DESIGN EQUATIONS

The sensor design equations developed in Chapter 3 will now be used to optimize a sensor design for a simple module under test and to evaluate the tradeoffs which exist for this circuit between the module size, the error current resolution, and the testing cycle time.

The first step in the design process is to establish values (and perhaps tolerances) for all of the needed circuit parameters. The circuit parameters which will be used for this example are listed in Table 4.1. Note that each parameter has both an expected value and a relative tolerance.

Table 4.1 Basic parameters for simple circuit example.

	Expected Value	Tolerance
Is	1e–16	100%
vt	26e–3	1%
k*	20e–6	5%
C	10e–12	5%

* Note : k is defined for a unit size transistor.

The tester cycle time in this example will be considered to be bounded by T_{min} = 15 ns and T_{max} = 20 ns and, to account for uncertainty in the design, the required voltage margin (*RVM*) will be set at 0.1 V. The leakage current for this module is guaranteed to be no more than 20 uA and the desired error current resolution is 160 uA.

Figure 4.1 shows the design space for this circuit (using only the expected values of the circuit parameters) when no bias transistor is included. Note that, with k = 0 uA/V^2, it is impossible to design a sensor for this circuit which can meet the *RVM* of 0.1 V, given that I_{eo} is 20 uA. In fact, for the given values of T_{min} and T_{max}, it appears that the available voltage margin (*AVM*) is only about 0.037 V.

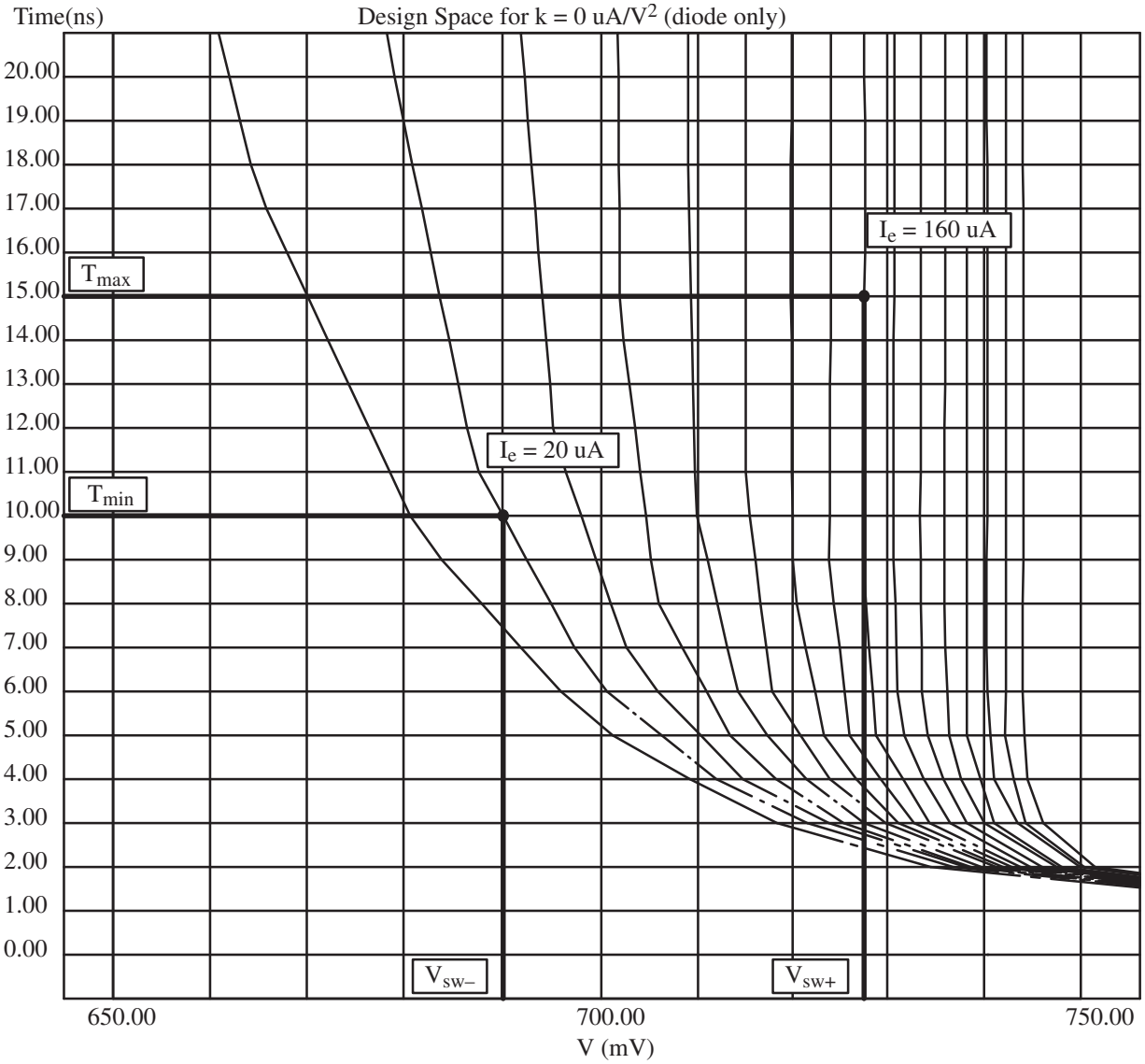

Figure 4.1 Design space for k = 0 uA/V^2. Note the curves representing I_{eo} and I_{err}. For the indicated values of T_{min} and T_{max}, the available voltage margin is around 0.037 V.

When the bias transistor is sized such that k = 60 uA/V^2, a design space similar to Figure 4.2 results. However, it turns out that the *AVM* is only slightly better at around 0.07 V. The question then arises as to whether there exists any value of k for which the *AVM* is greater than the *RVM*. The best means of determining this is to simply plot the *AVM* as a function of k. Figure 4.3 shows just such a plot.

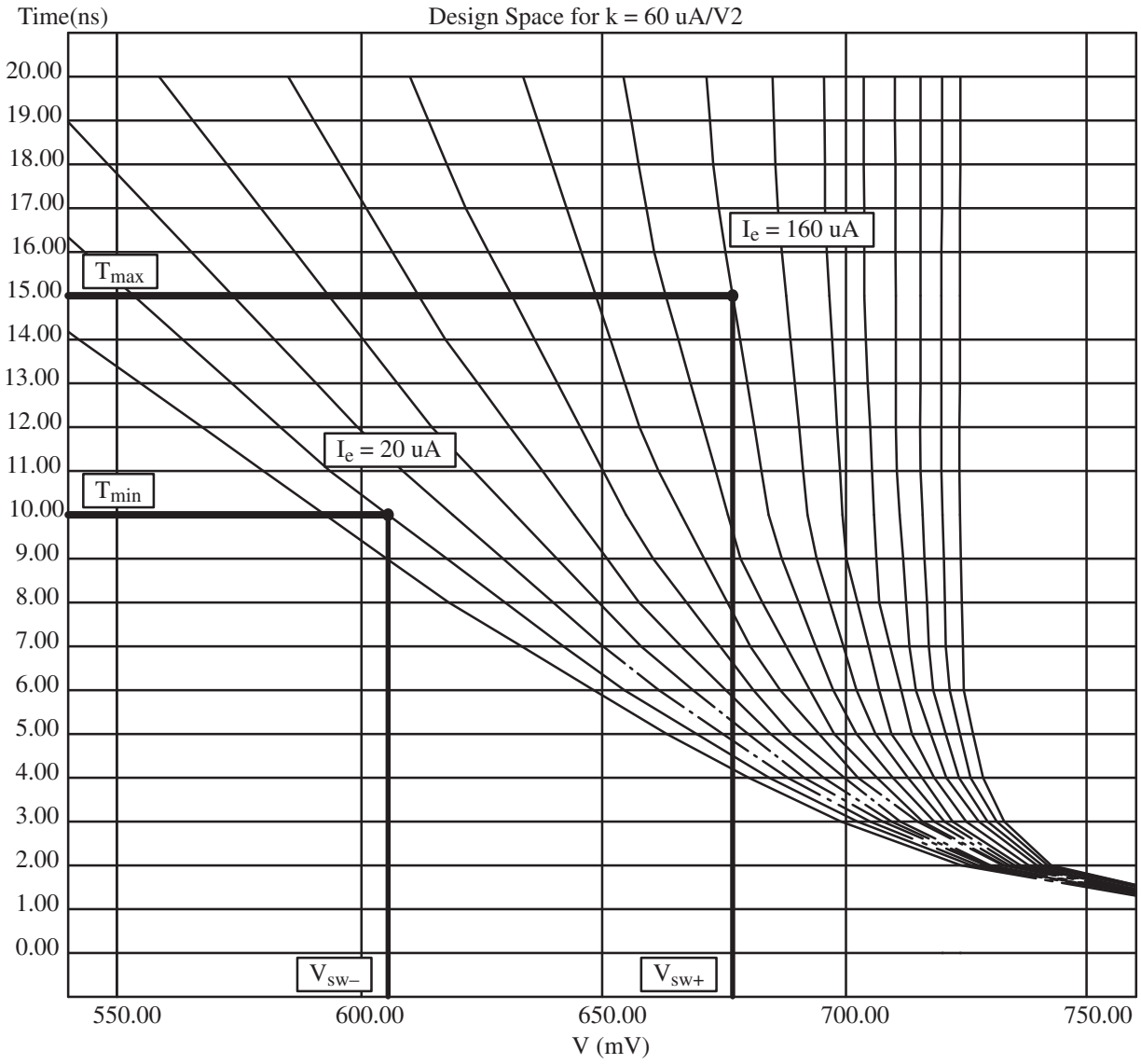

Figure 4.2 Design space for k = 60 uA/V^2. Note again the curves representing I_{eo} and I_{err}. For the indicated values of T_{min} and T_{max}, the available voltage margin is around 0.07 V.

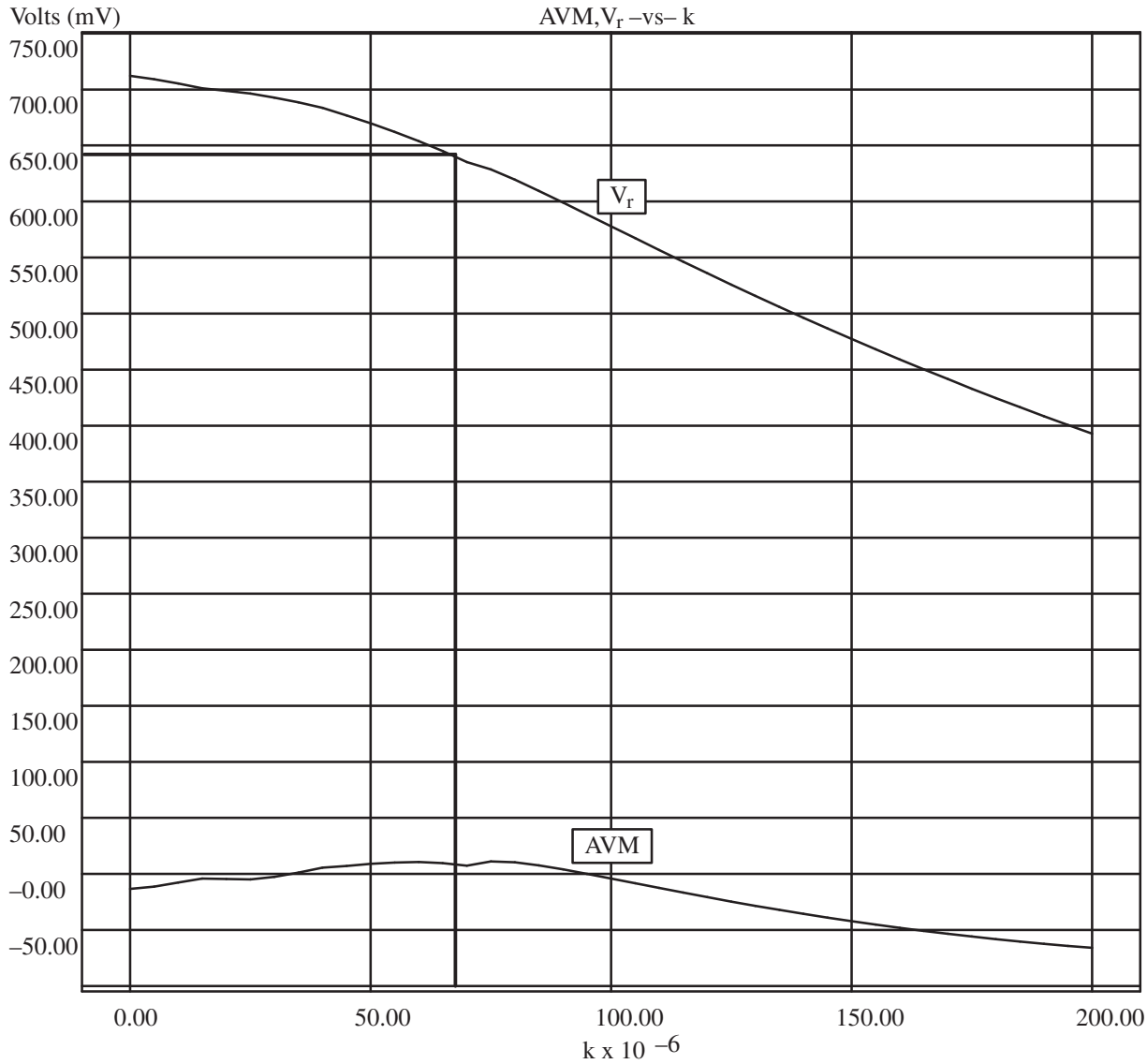

Figure 4.3 *AVM* and V_r –vs– k (base). Note that *AVM* appears to have a maximum value of around 0.02 V at k = 70 uA/V^2 with reference voltage of 0.64 V (under worst–case tolerances).

Note that there exists a point at which the *AVM* attains a maximum value. As k is increased beyond this value, the *AVM* decreases. However, the maximum value of the *AVM* appears to be only about 0.02 V, much less than the 0.1 V required. (Figure 4.3 is derived using worst-case parameter tolerances, so the results cannot be directly compared to Figures 4.1 and 4.2). It would appear, then, that it is impossible to design a sensor for this circuit which meets all of the stated requirements. It is at this point, then, that a tradeoff must be made.

Figure 4.4 shows the results of relaxing the requirements on the error current resolution from 120 uA to 300 uA. Note that there now exists a range of k for which the *AVM* is greater than the 0.1 V of required margin. This figure also indicates that there exists an optimal design at around k = 125 uA/V^2 and a voltage reference of V_r = 0.58 V which provides the maximum possible available voltage margin.

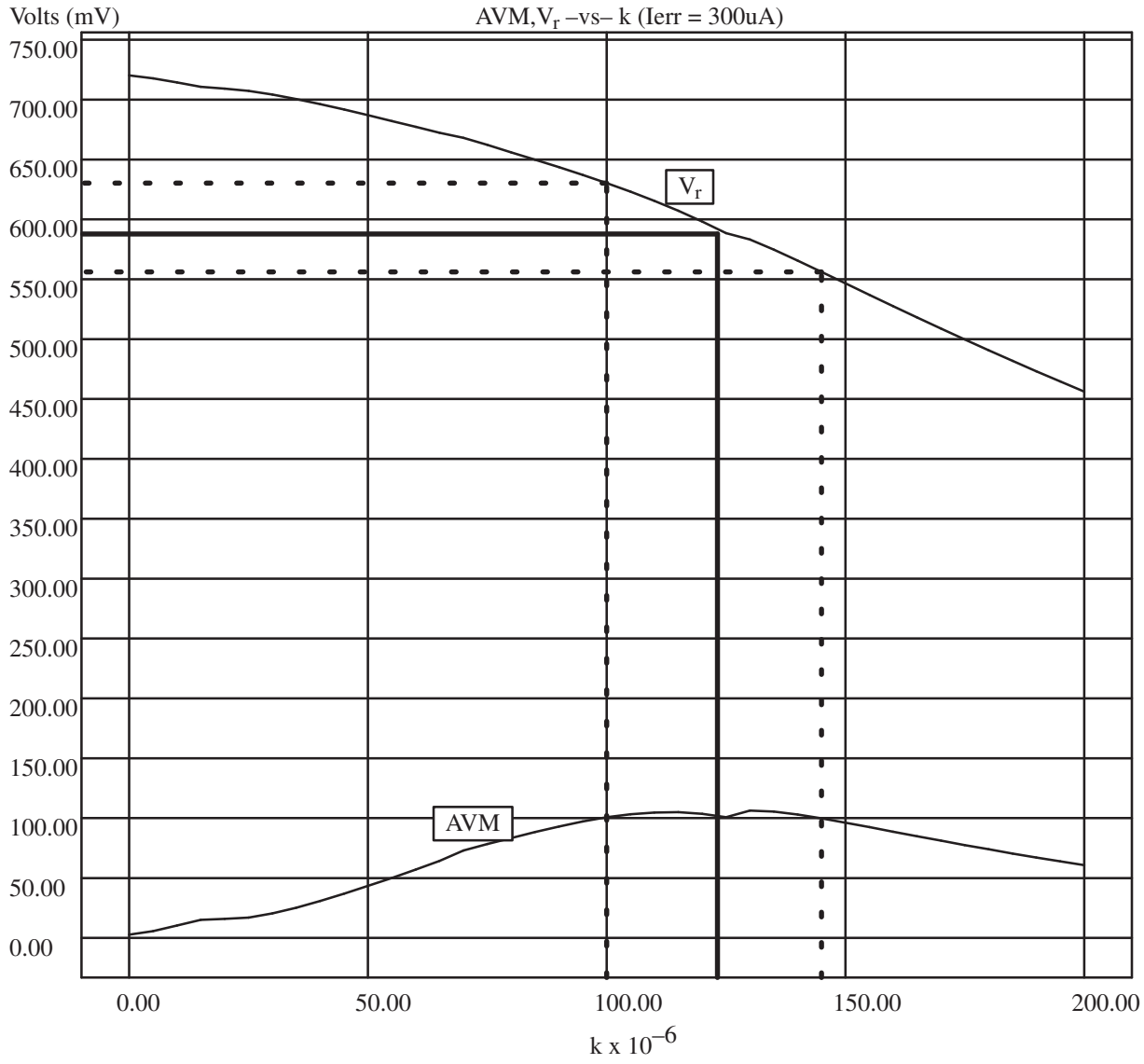

Figure 4.4 *AVM* and V_r –vs– k (I_{err} = 300uA).

If instead of relaxing the required error current resolution, the module size is decreased so that C = 5 pF, Figure 4.5 shows that an optimal sensor design exists at around k = 65 uA/V^2 and a voltage reference of V_r = 0.575 V.

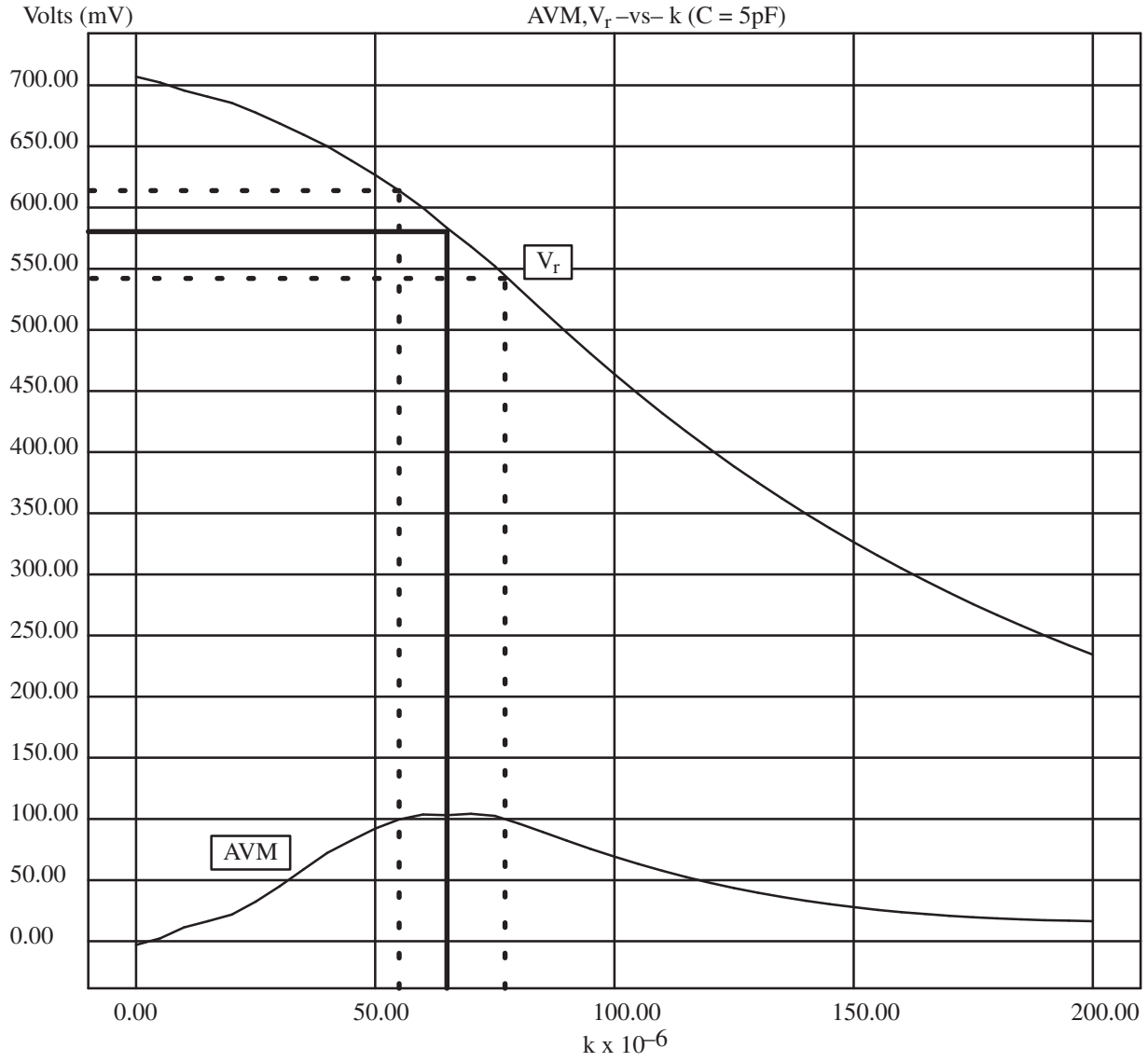

Figure 4.5 *AVM* and V_r –vs– k (C = 5pF).

Figure 4.6 shows the impact of increasing the length of the test cycle. For T_{min} = 20 ns and T_{msx} = 25 ns, it should be possible to construct an optimal sensor with k = 75 uA/V^2 and with V_r = 0.56 V.

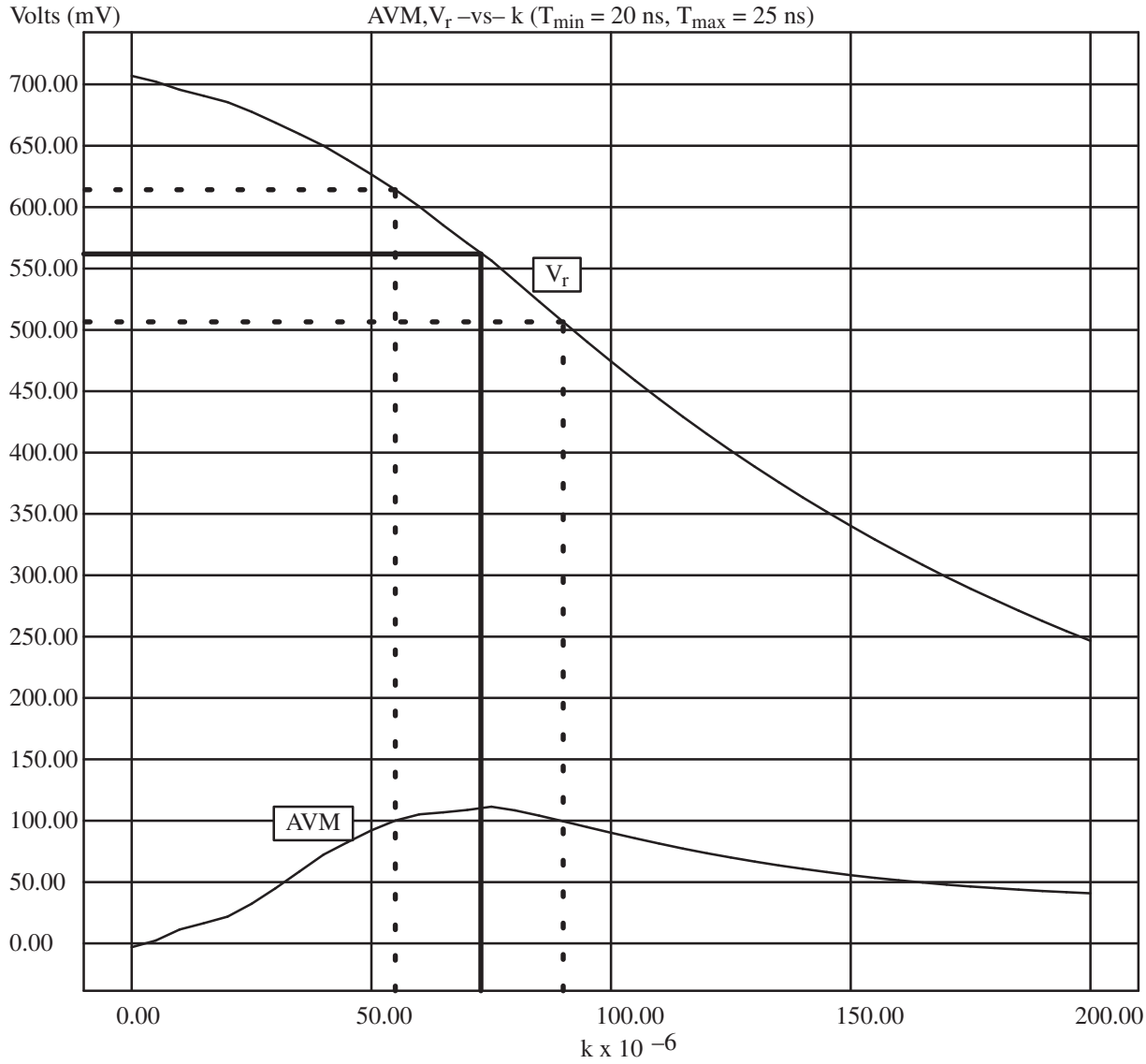

Figure 4.6 *AVM* and V_r –vs– k (T_{min} = 20 ns and T_{max} = 25 ns).

Although this particular example has been based on a specific circuit, it will always be true in general that there will exist a strict tradeoff between the module size, the tester cycle length, and the error current resolution. This simply means that there are no values of C, I_{err}, or T_{min} for which the *AVM* is a maximum; the *AVM* can always be improved by either increasing or decreasing one

of these three parameters. It will also be true that improving the circuit parameter tolerances and reducing T_{max} will improve the *AVM*.

The dependence of *AVM* on *k*, however, is not so simple. It is obvious from the above example that a value of *k* may exist for which the *AVM* reaches a maximum value. This implies that *k* is an important design parameter which can be optimized based on the circuit under test. It is interesting to note that designs which do not use a bias transistor are completely at the mercy of the required voltage margin. With a bias transistor, even a relatively large *RVM* can be accommodated. In designs where $k = 0$ uA/V^2, however, if the *RVM* is greater than the *AVM* for all values of I_{err} and T_{min} (as in Figure 4.1), the sensor designer is essentially out of luck.

Designs which rely completely on the bias transistor as the sensing element (no diode) also face some difficulties. When a sensor relies on only an MOS transistor as a sensing element, that transistor must be sized large enough to allow transient currents to pass without unreasonable degradation of the power supplies. However, it is also the value of *k* (the size of the transistor) which determines the *AVM* and, as previously demonstrated, large values of *k* may result in small values of *AVM*. This inherent conflict between the current carrying capability of the bias transistor and the resolution of the sensor has a negative impact on the scalability of MOS-based sensors. Because larger modules require larger bias transistors and because the *AVM* of the sensor must be at least equal to the *RVM*, the size of the module which can be tested by such a sensor is limited by the *RVM*.

5. CONCLUSIONS AND FUTURE WORK

The intent of this thesis has been to develop analytical guidelines for use in the design of current sensors for Iddq testing. Through simple circuit analysis, a set of equations was derived which related the sensor delay to basic circuit parameters. These delay equations were verified using Spice and then were used to derive a set of design equations which are applicable to a wide variety of sensor designs. Finally, these equations were used to design a simple sensor circuit and to verify the existence of a tradeoff between the resolution of the current sensor, the operating speed of the sensor, and the size of the module upon which the sensor is expected to operate.

A test chip has been fabricated to allow further verification of the results presented in this thesis. Statistical data obtainable from this chip should help to support the relationships derived in this thesis between the module size, the bias current, the diode saturation current, the magnitude of the error current, the reference voltage, and the resulting sensor delay. Included in the test chip are a number of different modules of different sizes with sensor diodes of various areas. This test chip should be capable of measuring the delay of the modules under test and the subsequent delay of the current sensors associated with them. It should also be possible to program different values for the bias currents, error currents, and voltage references by writing to registers on the chip. Upon completion of the fabrication process, this chip will provide accurate values for the diode saturation current and improved transistor models. This will allow a more direct comparison with the analytical results and the Spice simulations. The chip will also allow a better analysis of the impact of noise and temperature upon the switching thresholds of the current sensor.

APPENDIX A. IMPROVED DELAY EQUATION

The assumption made in deriving (2.26) was that the diode current below V_1 is negligible. This assumption is conservative in that, by neglecting the current contribution of the diode in the region near V_1, the calculated delay time will be somewhat pessimistic when compared to the actual value. There does, however, exist an approximation based on retaining an exponential current term which provides very accurate results, even in the region of V_1. This approximation takes the following form

$$\int_{T_1}^{t} d\tau = -C \int_{V_1}^{v} \left[\frac{1}{4k * v - \left(\frac{k}{2}\right) * v^2 - I_e} + \frac{1}{I_s * \exp\left[\frac{v}{v_t}\right] + I_1} - \frac{1}{I_1} \right] * dv$$

This integration can be done in parts, with the difficult integrals having already been evaluated in Chapter 2. Integrating and evaluating the remaining constant term and then multiplying the result by (v_t/v_t) gives

$$-C \int_{V_1}^{v} -\frac{dv}{I_1} = -\left[\frac{C * v_t}{I_1}\right]\left(\frac{V_1 - v}{v_t}\right)$$

When this result is added to the integral of the exponential term, (2.13), the terms linear in v drop out, leaving only

$$\left(\frac{C * v_t}{I_1}\right) \ln\left[\frac{I_1 + I_s * \exp\left[\frac{v}{v_t}\right]}{I_1 + I_s * \exp\left[\frac{V_1}{v_t}\right]}\right]$$

Adding this result to the solution for the polynomial expression, (2.26), results in

$$t = T_1 + \left(\frac{2C}{k\,(r_2 - r_1)}\right) \ln\left[\frac{(v - r_2)(V_1 - r_1)}{(v - r_1)(V_1 - r_2)}\right] + \left(\frac{C * v_t}{I_1}\right) \ln\left[\frac{I_1 + I_s * \exp\left[\frac{v}{v_t}\right]}{I_1 + I_s * \exp\left[\frac{V_1}{v_t}\right]}\right]$$

It is this expression which was used in generating curves for the figures in Chapter 2. This expression, however, cannot be solved for v in terms of t. Thus, the design equations derived in Chapter 3 rely solely on (2.26).

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